

Fig. 1

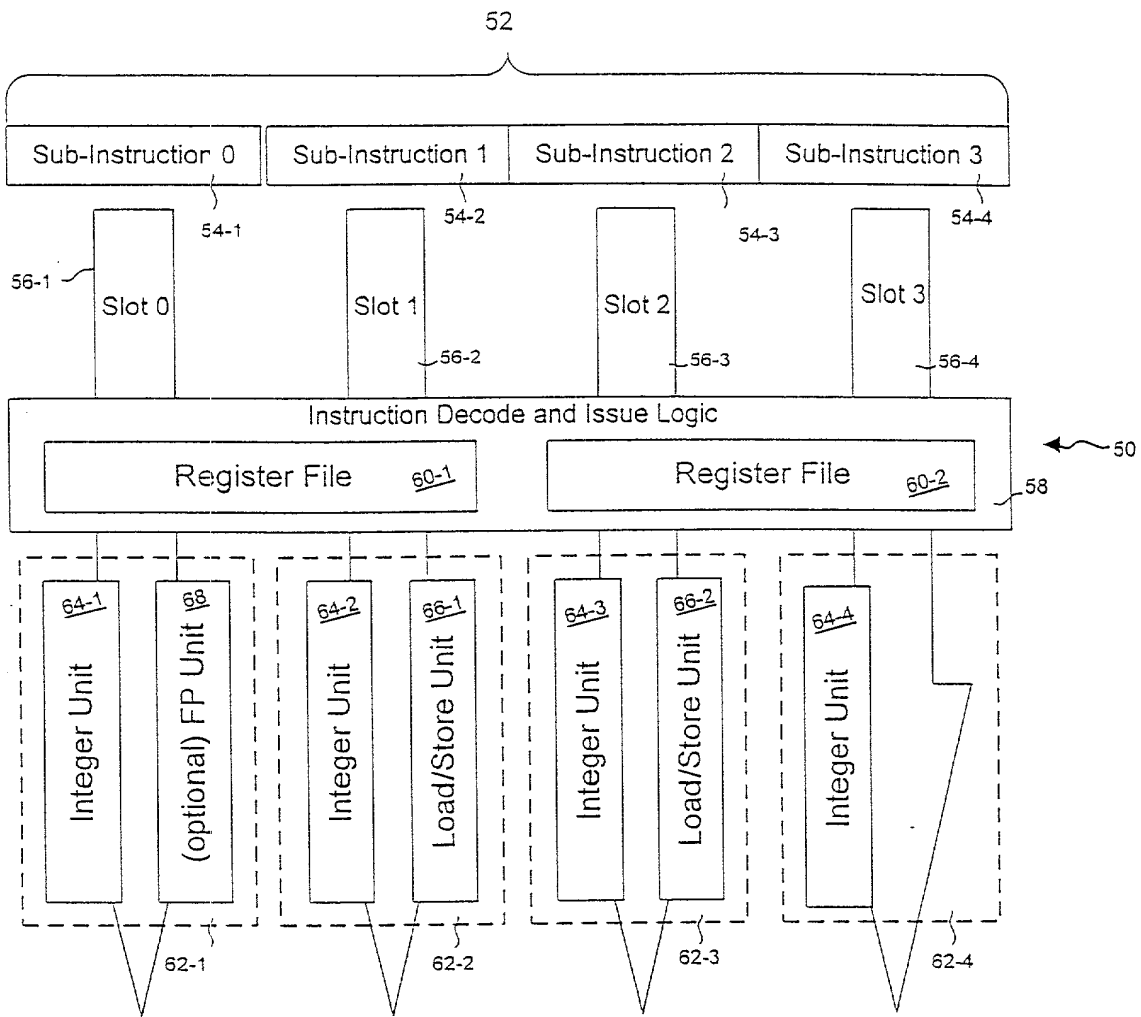


Fig. 2

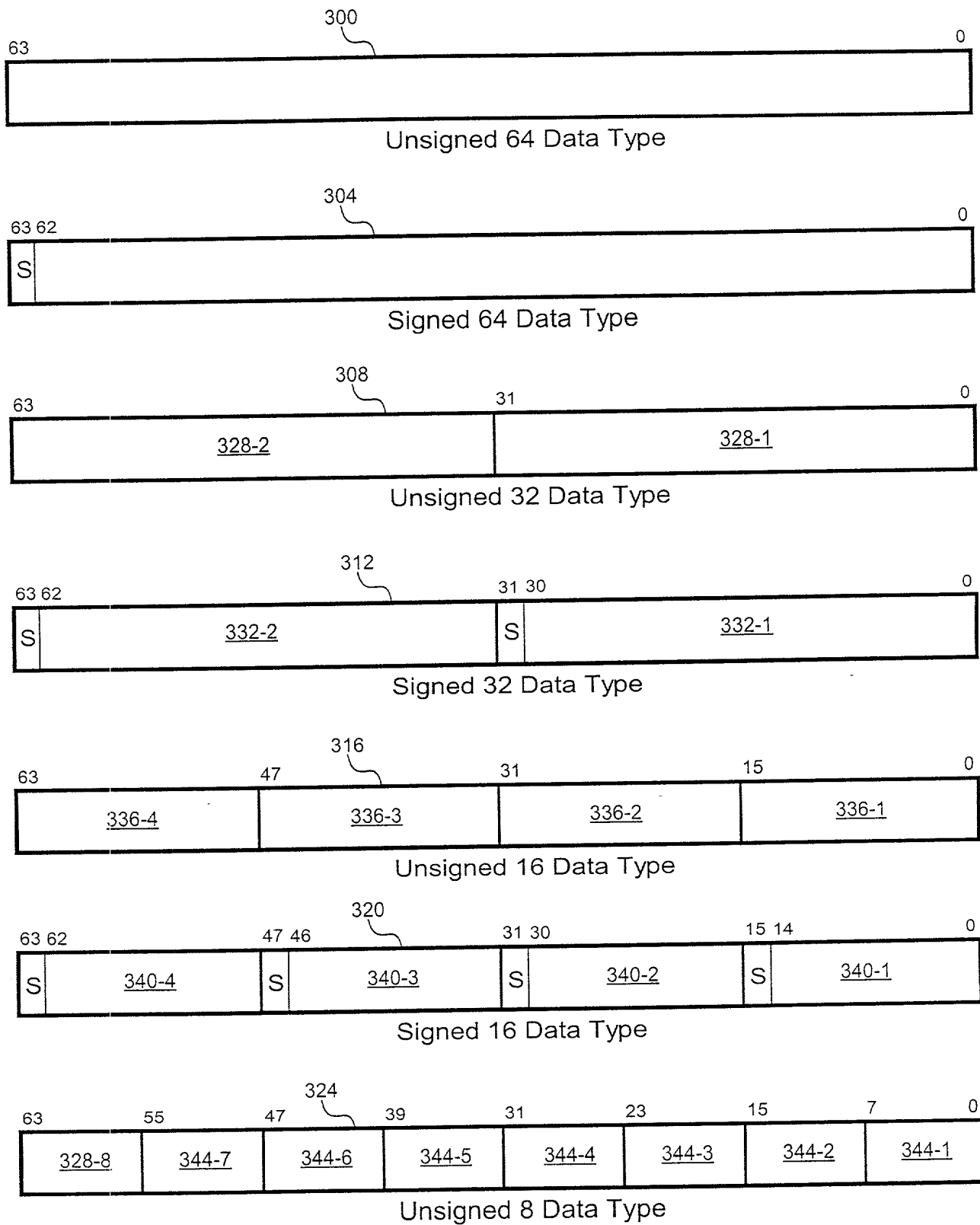
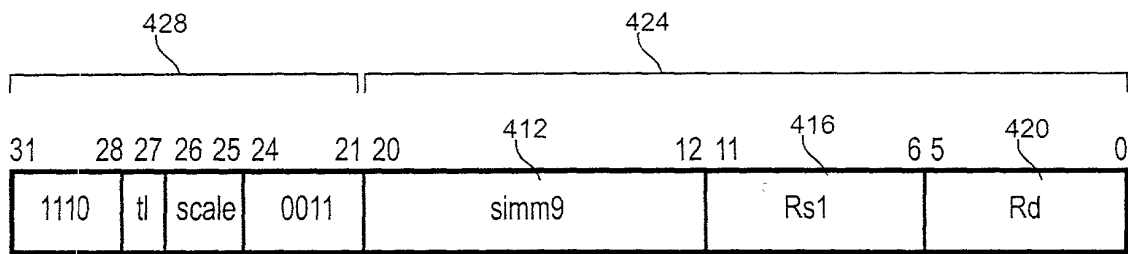
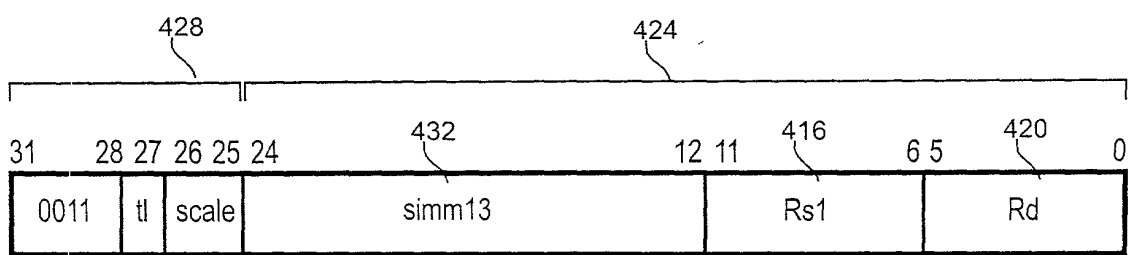


Fig. 3



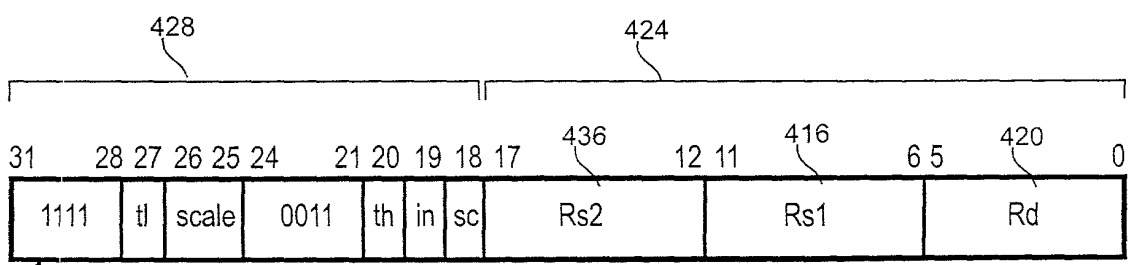
PADD simm9 Sub-Instruction: 8 and 16 bit Operands

400



PADD simm13 Sub-Instruction: 32 and 64 bit Operands

404



PADD Register Sub-Instruction: 8, 16, 32, and 64 bit Operands

408

Fig. 4

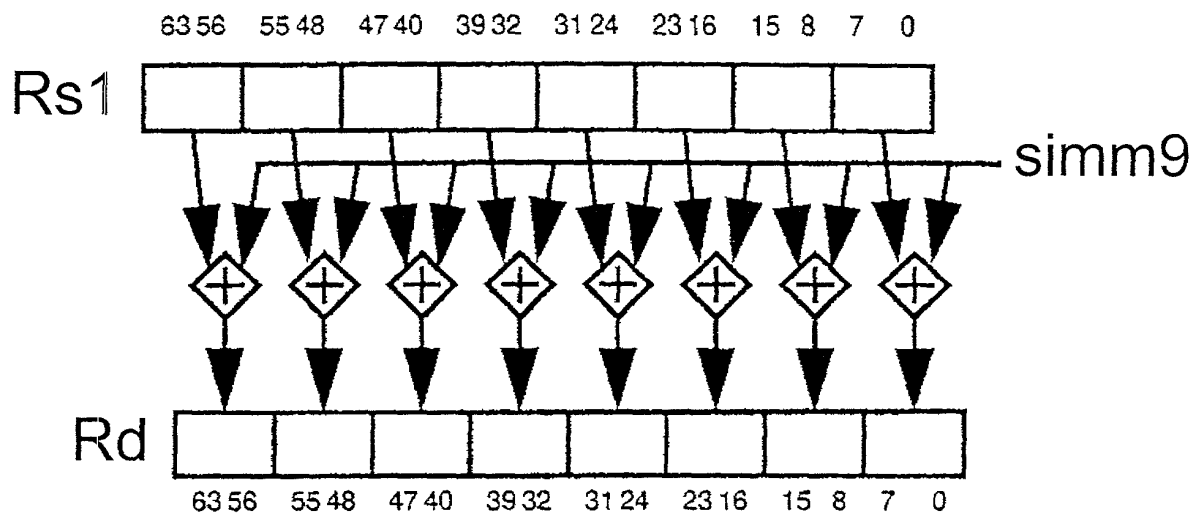


Fig. 5

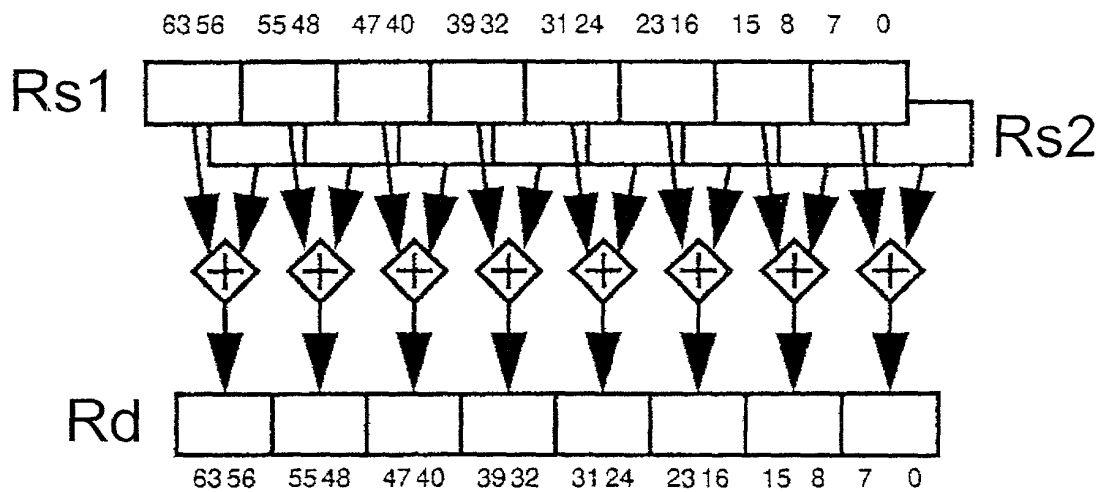


Fig. 6

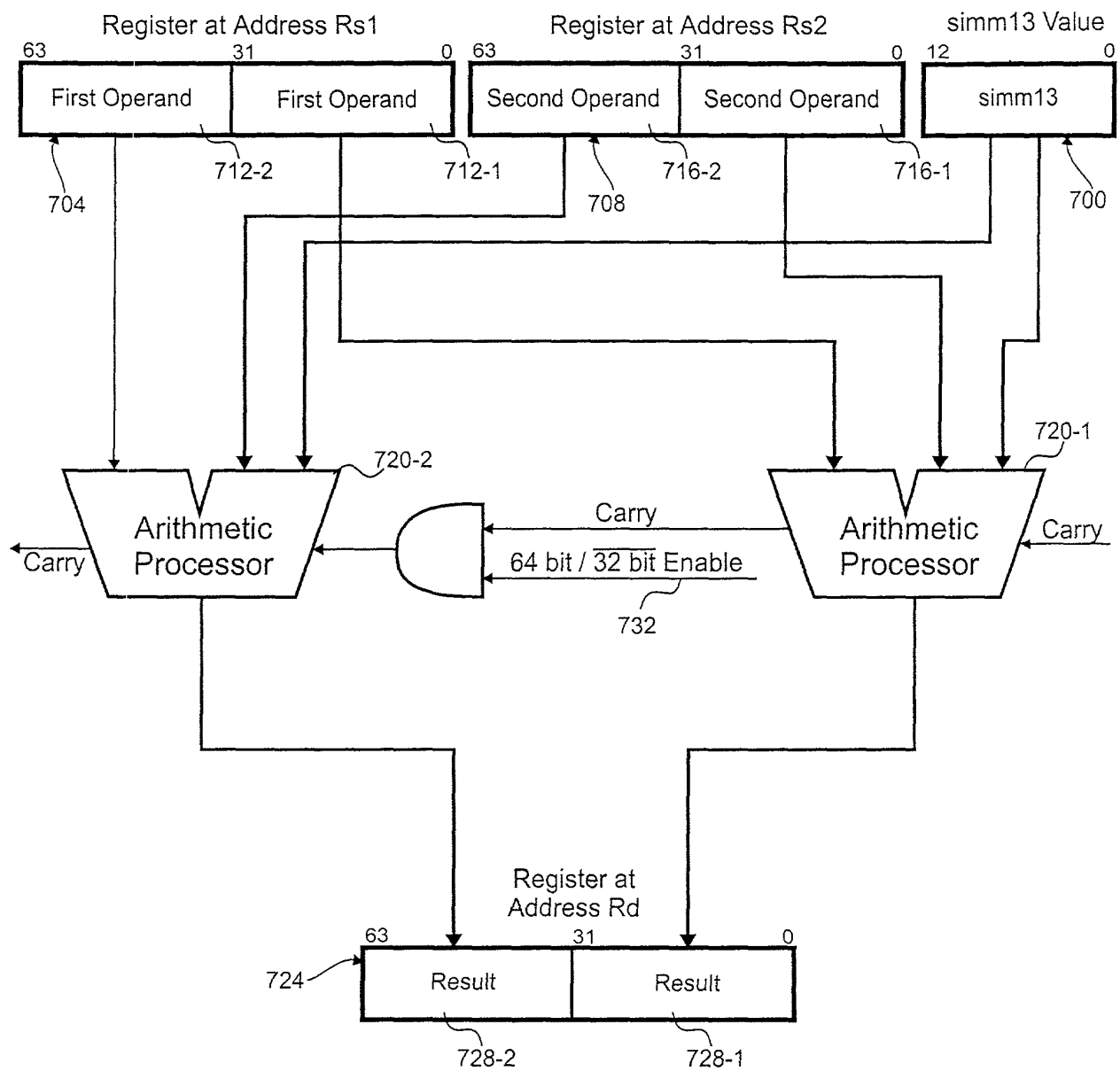


Fig. 7

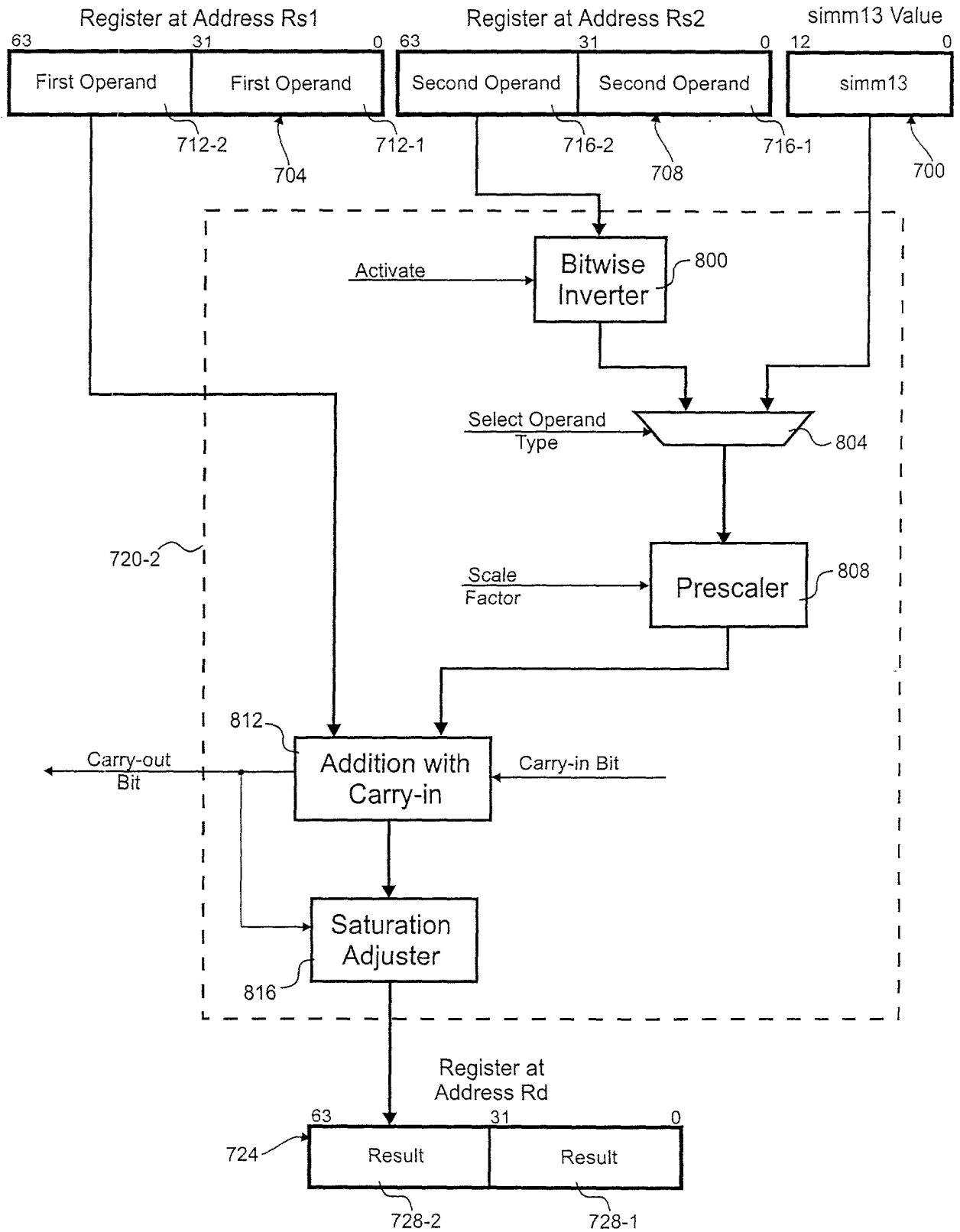


Fig. 8A

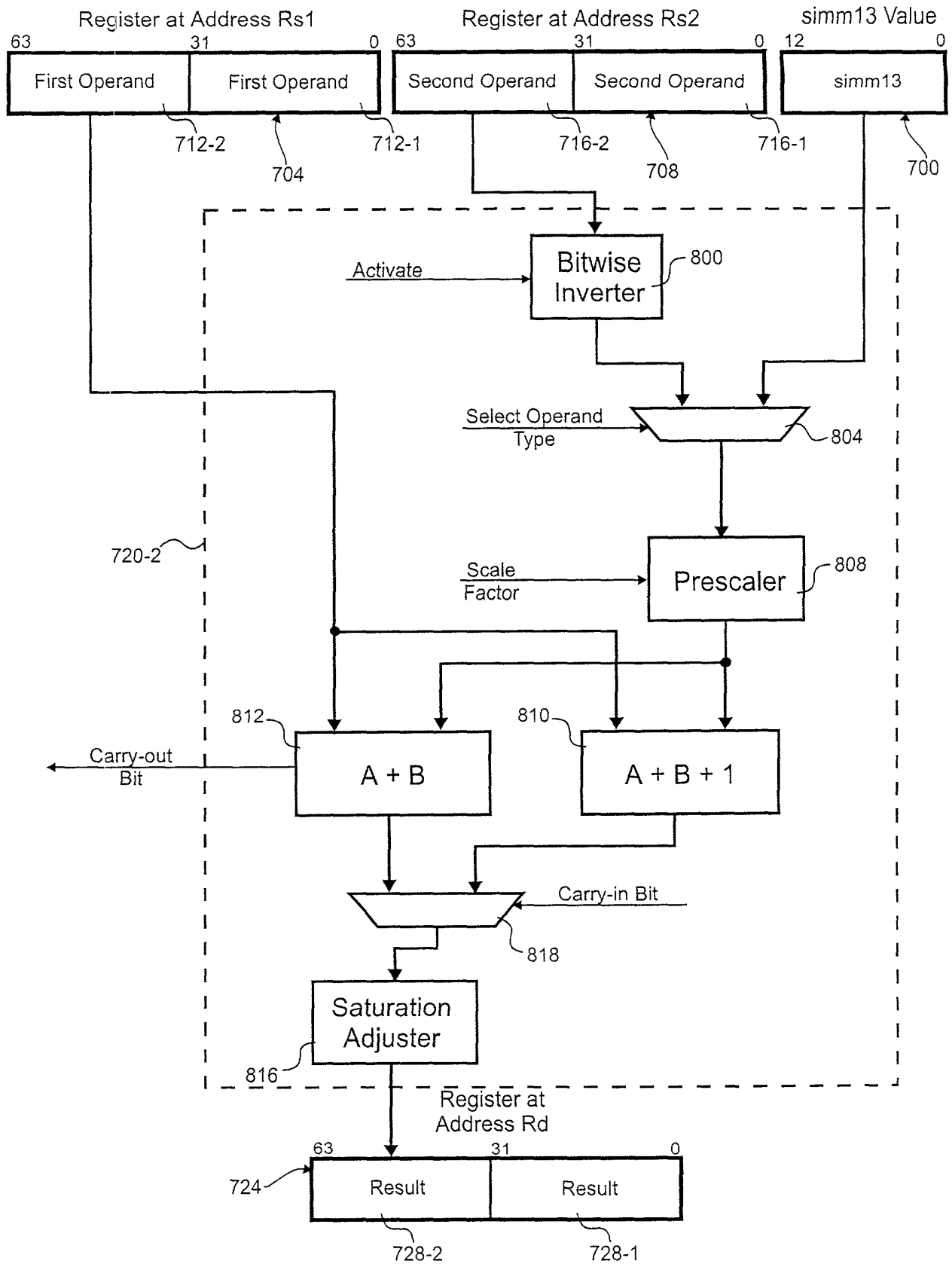


Fig. 8B



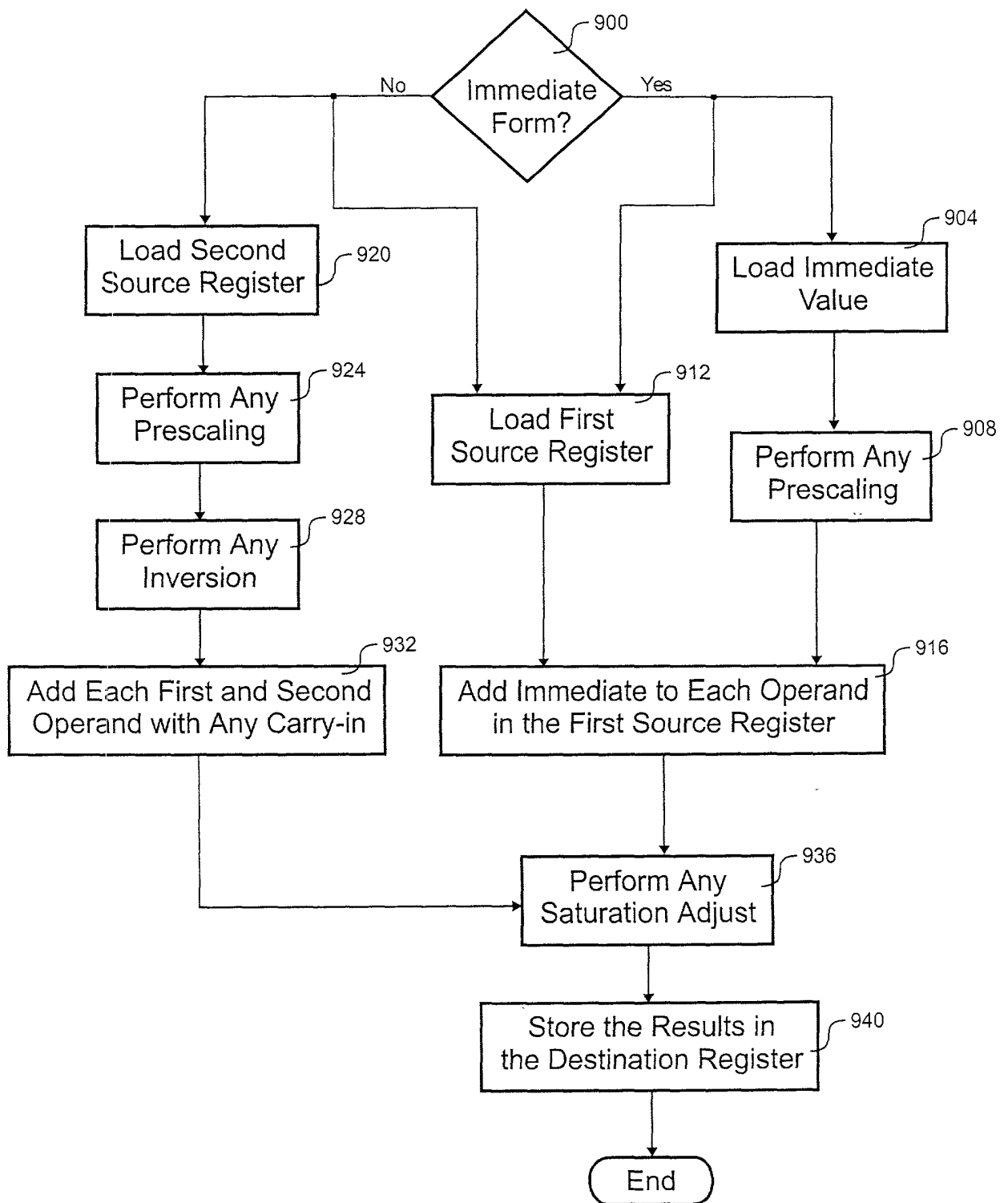


Fig. 9